

TL081, TL081A, TL081B, TL082, TL082A, TL082B TL084, TL084A, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS081G – FEBRUARY 1977 – REVISED SEPTEMBER 2004

- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion . . . 0.003% Typ
- High Input Impedance . . . JFET-Input Stage
- Latch-Up-Free Operation
- High Slew Rate . . . 13 V/ μ s Typ
- Common-Mode Input Voltage Range Includes V_{CC+}

description/ordering information

The TL08x JFET-input operational amplifier family is designed to offer a wider selection than any previously developed operational amplifier family. Each of these JFET-input operational amplifiers incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit. The devices feature high slew rates, low input bias and offset currents, and low offset-voltage temperature coefficient. Offset adjustment and external compensation options are available within the TL08x family.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The Q-suffix devices are characterized for operation from –40°C to 125°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

ORDERING INFORMATION

T_J	V_{IOmax} AT 25°C	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
0°C to 70°C	15 mV	PDIP (P)	Tube of 50	TL081CP	TL081CP
			Tube of 50	TL082CP	TL082CP
		PDIP (N)	Tube of 25	TL084CN	TL084CN
		SOIC (D)	Tube of 75	TL081CD	TL081C
			Reel of 2500	TL081CDR	
			Tube of 75	TL082CD	TL082C
			Reel of 2500	TL082CDR	
			Tube of 50	TL084CD	TL084C
			Reel of 2500	TL084CDR	
		SOP (PS)	Reel of 2000	TL081CPSR	T081
			Reel of 2000	TL082CPSR	T082
		SOP (NS)	Reel of 2000	TL084CNSR	TL084
		TSSOP (PW)	Tube of 150	TL082CPW	T082
			Reel of 2000	TL082CPWR	
			Tube of 90	TL084CPW	T084
			Reel of 2000	TL084CPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL084, TL084A, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS081G – FEBRUARY 1977 – REVISED SEPTEMBER 2004

description/ordering information (continued)

ORDERING INFORMATION

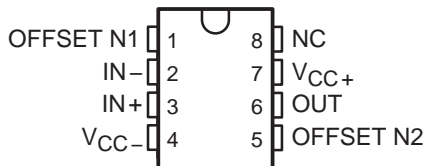
T _J	V _{IO} max AT 25°C	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
0°C to 70°C	6 mV	PDIP (P)	Tube of 50	TL081ACP	TL081ACP
			Tube of 50	TL082ACP	TL082ACP
		PDIP (N)	Tube of 25	TL084ACN	TL084ACN
		SOIC (D)	Tube of 75	TL081ACD	081AC
			Reel of 2500	TL081ACDR	
			Tube of 75	TL082ACD	082AC
			Reel of 2500	TL082ACDR	
		SOIC (D)	Tube of 50	TL084ACD	TL084AC
	Reel of 2500		TL084ACDR		
	SOP (PS)	Reel of 2000	TL082ACPSR	T082A	
	SOP (NS)	Reel of 2000	TL084ACNSR	TL084A	
	3 mV	PDIP (P)	Tube of 50	TL081BCP	TL081BCP
			Tube of 50	TL082BCP	TL082BCP
		PDIP (N)	Tube of 25	TL084BCN	TL084BCN
		SOIC (D)	Tube of 75	TL081BCD	081BC
			Reel of 2500	TL081BCDR	
Tube of 75			TL082BCD	082BC	
Reel of 2500			TL082BCDR		
SOIC (D)		Tube of 50	TL084BCD	TL084BC	
	Reel of 2500	TL084BCDR			
-40°C to 85°C	6 mV	PDIP (P)	Tube of 50	TL081IP	TL081IP
			Tube of 50	TL082IP	TL082IP
		PDIP (N)	Tube of 25	TL084IN	TL081IN
		SOIC (D)	Tube of 75	TL081ID	TL081I
			Reel of 2500	TL081IDR	
			Tube of 75	TL082ID	TL082I
			Reel of 2500	TL082IDR	
		SOIC (D)	Tube of 50	TL084ID	TL084I
			Reel of 2500	TL084IDR	
		TSSOP (PW)	Reel of 2000	TL082IPWR	Z082
-40°C to 125°C	9 mV	SOIC (D)	Tube of 50	TL084QD	TL084QD
			Reel of 2500	TL084QDR	
-55°C to 125°C	9 mV	CDIP (J)	Tube of 25	TL084MJ	TL084MJ
		LCCC (FK)	Reel of 55	TL084FK	TL084FK
	6 mV	CDIP (JG)	Tube of 50	TL082MJG	TL082MJG
		LCCC (FK)	Tube of 55	TL082MFK	TL082MFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

TL081, TL081A, TL081B, TL082, TL082A, TL082B TL084, TL084A, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

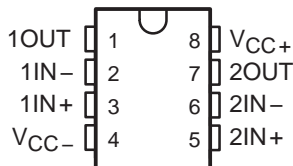
SLOS081G – FEBRUARY 1977 – REVISED SEPTEMBER 2004

TL081, TL081A, TL081B
D, P, OR PS PACKAGE
(TOP VIEW)

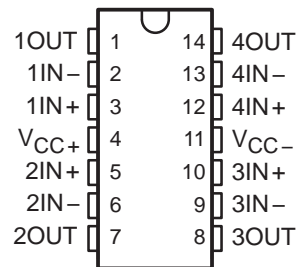


NC – No internal connection

TL082, TL082A, TL082B
D, JG, P, PS, OR PW PACKAGE
(TOP VIEW)



TL084, TL084A, TL084B
D, J, N, NS, OR PW PACKAGE
(TOP VIEW)

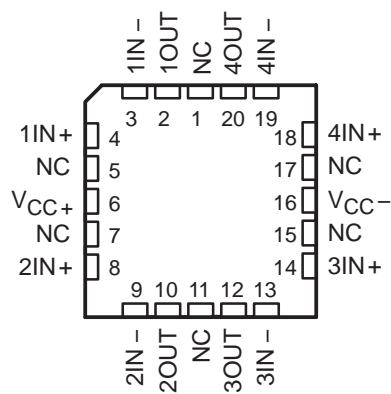


TL082M . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

TL084M . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

symbols



**TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL084, TL084A, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS081G – FEBRUARY 1977 – REVISED SEPTEMBER 2004

schematic (each amplifier)



Component values shown are nominal.

TL081, TL081A, TL081B, TL082, TL082A, TL082B TL084, TL084A, TL084B JFET-INPUT OPERATIONAL AMPLIFIERS

SLOS081G – FEBRUARY 1977 – REVISED SEPTEMBER 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

	TL08_C TL08_AC TL08_BC	TL08_I	TL084Q	TL08_M	UNIT
Supply voltage, V_{CC+} (see Note 1)	18	18	18	18	V
Supply voltage V_{CC-} (see Note 1)	-18	-18	-18	-18	V
Differential input voltage, V_{ID} (see Note 2)	± 30	± 30	± 30	± 30	V
Input voltage, V_I (see Notes 1 and 3)	± 15	± 15	± 15	± 15	V
Duration of output short circuit (see Note 4)	Unlimited	Unlimited	Unlimited	Unlimited	
Continuous total power dissipation	See Dissipation Rating Table				
Operating free-air temperature range, T_A	0 to 70	-40 to 85	-40 to 125	-55 to 125	°C
Package thermal impedance, θ_{JA} (see Notes 5 and 6)	D package (8-pin)	97	97		°C/W
	D package (14-pin)	86	86		
	N package (14-pin)	76	76		
	NS package (14-pin)	80			
	P package (8-pin)	85	85		
	PS package (8-pin)	95	95		
	PW package (8-pin)	149			
	PW package (14-pin)	113	113		
Operating virtual junction temperature	150	150	150	150	°C
Case temperature for 60 seconds, T_C	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J or JG package			300	°C
Storage temperature range, T_{stg}	-65 to 150	-65 to 150	-65 to 150	-65 to 150	°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
- All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 - Differential voltages are at $IN+$ with respect to $IN-$.
 - The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
 - The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
 - Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 - The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D (14 pin)	680 mW	7.6 mW/°C	60°C	604 mW	490 mW	186 mW
FK	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
J	680 mW	11.0 mW/°C	88°C	680 mW	680 mW	273 mW
JG	680 mW	8.4 mW/°C	69°C	672 mW	546 mW	210 mW



**TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL084, TL084A, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS081G – FEBRUARY 1977 – REVISED SEPTEMBER 2004

electrical characteristics, $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A †	TL081C TL082C TL084C			TL081AC TL082AC TL084AC			TL081BC TL082BC TL084BC			TL081I TL082I TL084I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	V _O = 0 R _S = 50 Ω	25°C Full range	3	15	6	3	6	2	3	3	6	3	6	mV	
α _{VIO}	V _O = 0 R _S = 50 Ω	Full range		20	7.5				5				9		
I _{IO}	V _O = 0	Full range	18			18			18			18		μV/°C	
I _{IB}	V _O = 0	25°C Full range	5	200	100	5	100	5	100	5	100	5	100	pA	
V _{ICR}	V _O = 0	Full range		2	2		2		2		2		10	nA	
V _{OM}	V _O = 0	25°C Full range	30	400	200	30	200	30	200	30	200	30	200	pA	
V _{ICR}	V _O = 0	Full range		10	7		7		7		7		20	nA	
V _{ICR}	Common-mode input voltage range	25°C	±11	-12 to 15		±11	-12 to 15		±11	-12 to 15		±11	-12 to 15	V	
V _{OM}	Maximum peak output voltage swing	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5	V	
A _{V/D}	Large-signal differential voltage amplification	Full range	±12			±12			±12			±12			
A _{V/D}	VO = ±10 V, R _L ≥ 2 kΩ	25°C	±10	±12		±10	±12		±10	±12		±10	±12	V/mV	
A _{V/D}	VO = ±10 V, R _L ≥ 2 kΩ	Full range	15			25			25			25			
B ₁	Unity-gain bandwidth	25°C	3			3			3			3		MHz	
r _i	Input resistance	25°C	10 ¹²			10 ¹²			10 ¹²			10 ¹²		Ω	
CMRR	Common-mode rejection ratio	25°C	70	86		75	86		75	86		75	86	dB	
k _{SVR}	Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO})	25°C	70	86		80	86		80	86		80	86	dB	
I _{CC}	Supply current (per amplifier)	25°C	1.4	2.8		1.4	2.8		1.4	2.8		1.4	2.8	mA	
V _{O1} /V _{O2}	Crosstalk attenuation	25°C	120			120			120			120		dB	

† All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range for T_A is 0°C to 70°C for TL08_C, TL08_AC, TL08_BC and -40°C to 85°C for TL08_I.

‡ Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 17. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.



**TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL084, TL084A, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS081G – FEBRUARY 1977 – REVISED SEPTEMBER 2004

electrical characteristics, $V_{CC\pm} = \pm 15\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	T_A	TL081M, TL082M			TL084Q, TL084M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 0, R_S = 50\ \Omega$	25°C	3	6		3	9	mV	
		Full range			9		15		
α_{VIO} Temperature coefficient of input offset voltage	$V_O = 0, R_S = 50\ \Omega$	Full range	18			18			$\mu\text{V}/^\circ\text{C}$
I_{IO} Input offset current‡	$V_O = 0$	25°C	5	100		5	100	pA	
		125°C	20			20			nA
I_{IB} Input bias current‡	$V_O = 0$	25°C	30	200		30	200	pA	
		125°C	50			50			nA
V_{ICR} Common-mode input voltage range		25°C	± 11	-12 to 15		± 11	-12 to 15	V	
V_{OM} Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	± 12	± 13.5		± 12	± 13.5	V	
	$R_L \geq 10\ \text{k}\Omega$	Full range	± 12		± 12				
	$R_L \geq 2\ \text{k}\Omega$		± 10	± 12	± 10	± 12			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L \geq 2\ \text{k}\Omega$	25°C	25	200		25	200	V/mV	
	$V_O = \pm 10\ \text{V}, R_L \geq 2\ \text{k}\Omega$	Full range	15		15				
B_1 Unity-gain bandwidth		25°C	3			3			MHz
r_i Input resistance		25°C	10^{12}			10^{12}			Ω
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, V_O = 0, R_S = 50\ \Omega$	25°C	80	86		80	86	dB	
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 15\ \text{V to } \pm 9\ \text{V}, V_O = 0, R_S = 50\ \Omega$	25°C	80	86		80	86	dB	
I_{CC} Supply current (per amplifier)	$V_O = 0, \text{ No load}$	25°C	1.4	2.8		1.4	2.8	mA	
V_{O1}/V_{O2} Crosstalk attenuation	$A_{VD} = 100$	25°C	120			120			dB

† All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.

‡ Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 17. Pulse techniques must be used that maintain the junction temperatures as close to the ambient temperature as possible.

operating characteristics, $V_{CC\pm} = \pm 15\ \text{V}, T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
SR Slew rate at unity gain	$V_I = 10\ \text{V}, R_L = 2\ \text{k}\Omega, C_L = 100\ \text{pF}, \text{ See Figure 1}$	8*	13		V/ μs	
	$V_I = 10\ \text{V}, R_L = 2\ \text{k}\Omega, C_L = 100\ \text{pF}, T_A = -55^\circ\text{C to } 125^\circ\text{C}, \text{ See Figure 1}$	5*				
t_r Rise time	$V_I = 20\ \text{mV}, R_L = 2\ \text{k}\Omega, C_L = 100\ \text{pF}, \text{ See Figure 1}$	0.05			μs	
Overshoot factor		20			%	
V_n Equivalent input noise voltage	$R_S = 20\ \Omega$	f = 1 kHz			$\text{nV}/\sqrt{\text{Hz}}$	
		f = 10 Hz to 10 kHz			μV	
I_n Equivalent input noise current	$R_S = 20\ \Omega, f = 1\ \text{kHz}$	0.01			$\text{pA}/\sqrt{\text{Hz}}$	
THD Total harmonic distortion	$V_{rms} = 6\ \text{V}, f = 1\ \text{kHz}$	$A_{VD} = 1, R_S \leq 1\ \text{k}\Omega, R_L \geq 2\ \text{k}\Omega,$	0.003			%

*On products compliant to MIL-PRF-38535, this parameter is not production tested.



**TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL084, TL084A, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS081G – FEBRUARY 1977 – REVISED SEPTEMBER 2004

operating characteristics, $V_{CC\pm} = \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR Slew rate at unity gain	$V_I = 10\text{ V}$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, See Figure 1	8	13		$\text{V}/\mu\text{s}$
t_r Rise time	$V_I = 20\text{ mV}$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, See Figure 1		0.05		μs
Overshoot factor			20		%
V_n Equivalent input noise voltage	$R_S = 20\ \Omega$	$f = 1\text{ kHz}$	18		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ Hz to } 10\text{ kHz}$	4		μV
I_n Equivalent input noise current	$R_S = 20\ \Omega$, $f = 1\text{ kHz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$
THD Total harmonic distortion	$V_{I\text{rms}} = 6\text{ V}$, $f = 1\text{ kHz}$, $A_{VD} = 1$, $R_S \leq 1\text{ k}\Omega$, $R_L \geq 2\text{ k}\Omega$,		0.003		%

PARAMETER MEASUREMENT INFORMATION

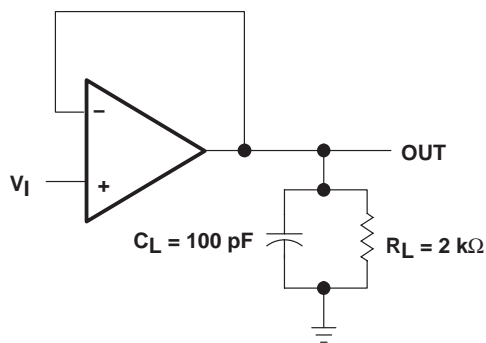


Figure 1

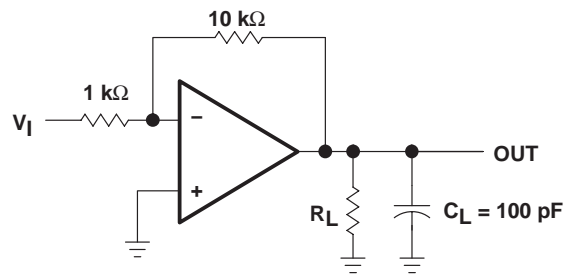


Figure 2

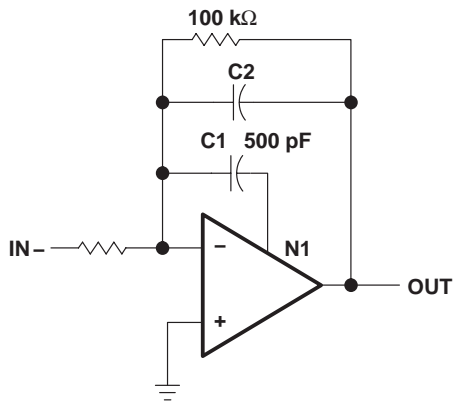


Figure 3

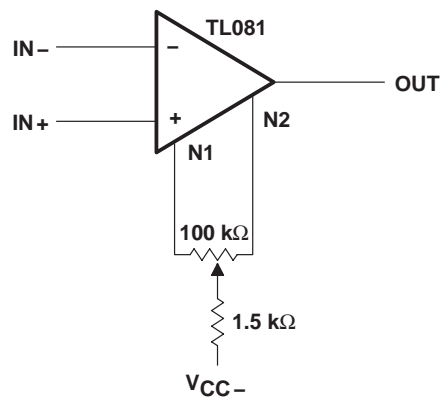


Figure 4

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
V _{OM}	Maximum peak output voltage	vs Frequency
		vs Free-air temperature
		vs Load resistance
		vs Supply voltage
AVD	Large-signal differential voltage amplification	vs Free-air temperature
		vs Frequency
	Differential voltage amplification	vs Frequency with feed-forward compensation
PD	Total power dissipation	vs Free-air temperature
I _{CC}	Supply current	vs Free-air temperature
		vs Supply voltage
I _{IB}	Input bias current	vs Free-air temperature
	Large-signal pulse response	vs Time
V _O	Output voltage	vs Elapsed time
CMRR	Common-mode rejection ratio	vs Free-air temperature
V _n	Equivalent input noise voltage	vs Frequency
THD	Total harmonic distortion	vs Frequency

**MAXIMUM PEAK OUTPUT VOLTAGE
 vs
 FREQUENCY**

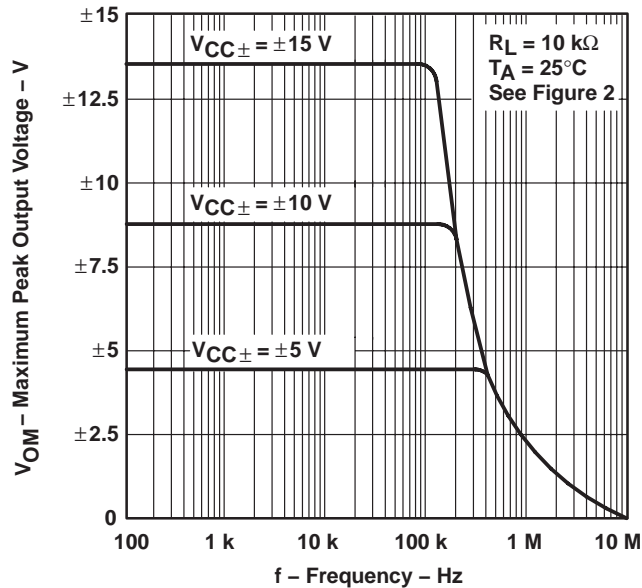


Figure 5

**MAXIMUM PEAK OUTPUT VOLTAGE
 vs
 FREQUENCY**

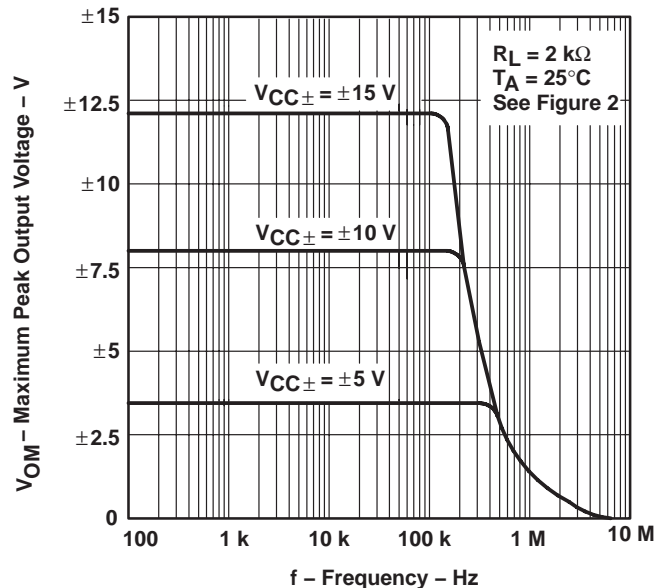


Figure 6

**TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL084, TL084A, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS081G – FEBRUARY 1977 – REVISED SEPTEMBER 2004

TYPICAL CHARACTERISTICS†

**MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY**

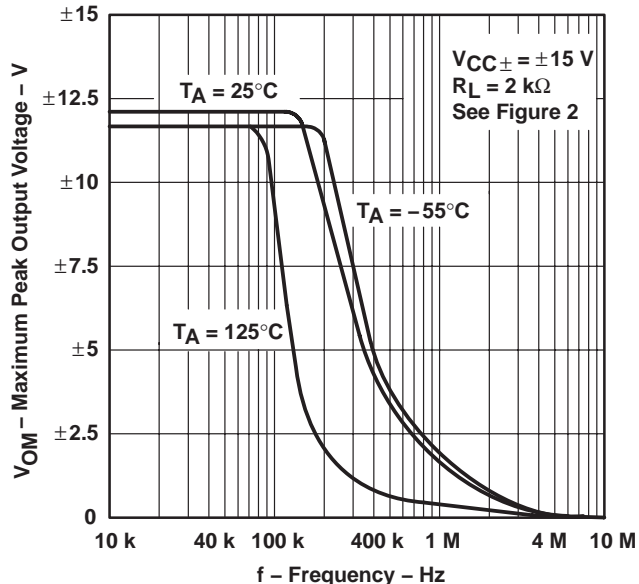


Figure 7

**MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE**

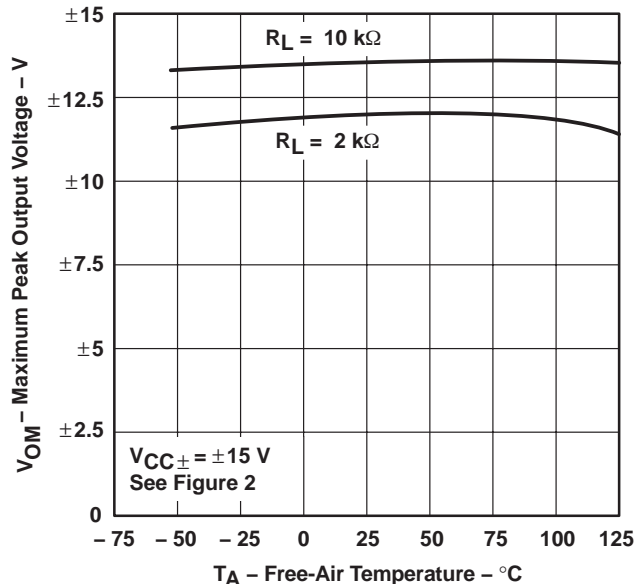


Figure 8

**MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE**

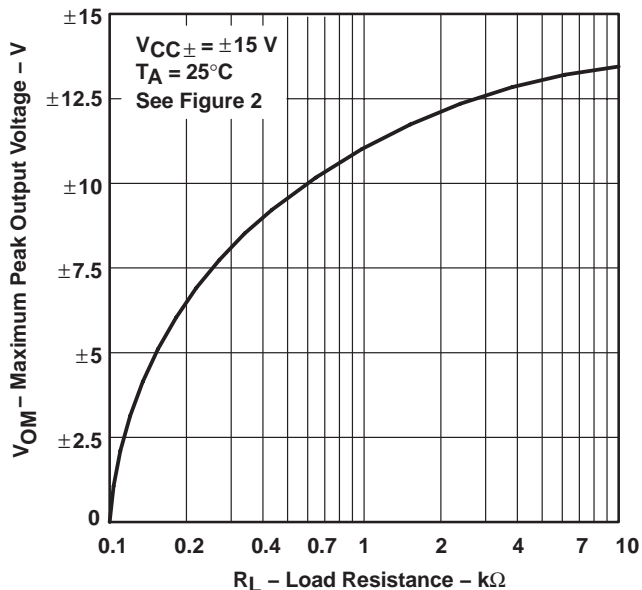


Figure 9

**MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE**

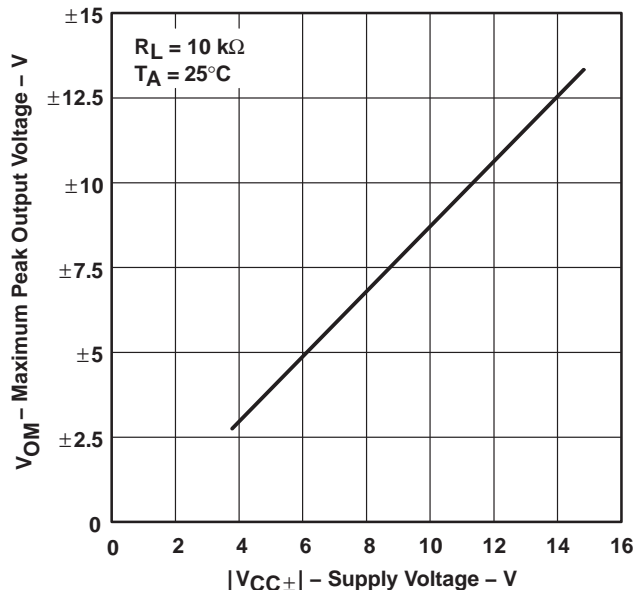


Figure 10

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS†

**LARGE-SIGNAL
 DIFFERENTIAL VOLTAGE AMPLIFICATION
 vs
 FREE-AIR TEMPERATURE**



Figure 11

**LARGE-SIGNAL
 DIFFERENTIAL VOLTAGE AMPLIFICATION
 vs
 FREQUENCY**

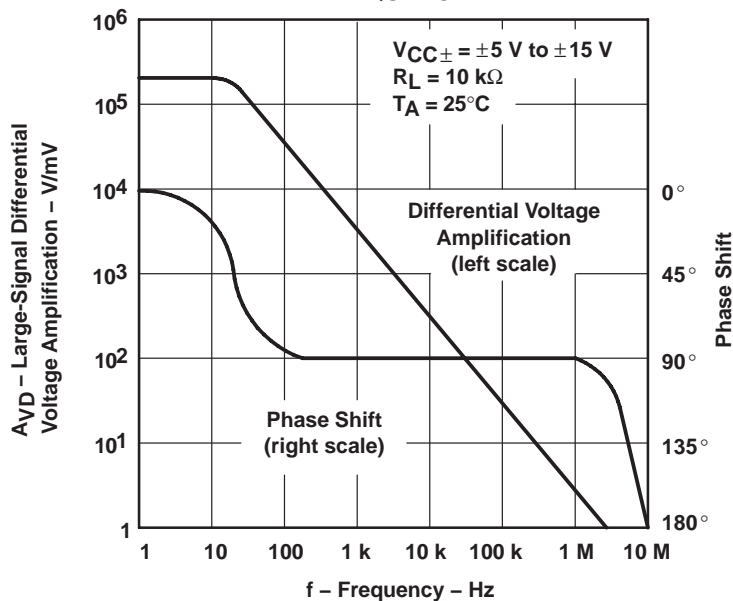


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL084, TL084A, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS081G – FEBRUARY 1977 – REVISED SEPTEMBER 2004

TYPICAL CHARACTERISTICS†

**DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREQUENCY WITH FEED-FORWARD COMPENSATION**



Figure 13

**TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE**



Figure 14

**SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE**



Figure 15

**SUPPLY CURRENT
vs
SUPPLY VOLTAGE**

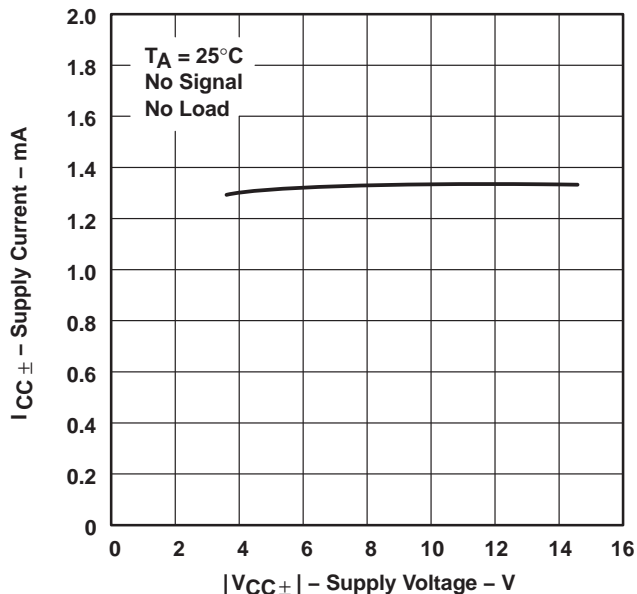


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS†



Figure 17

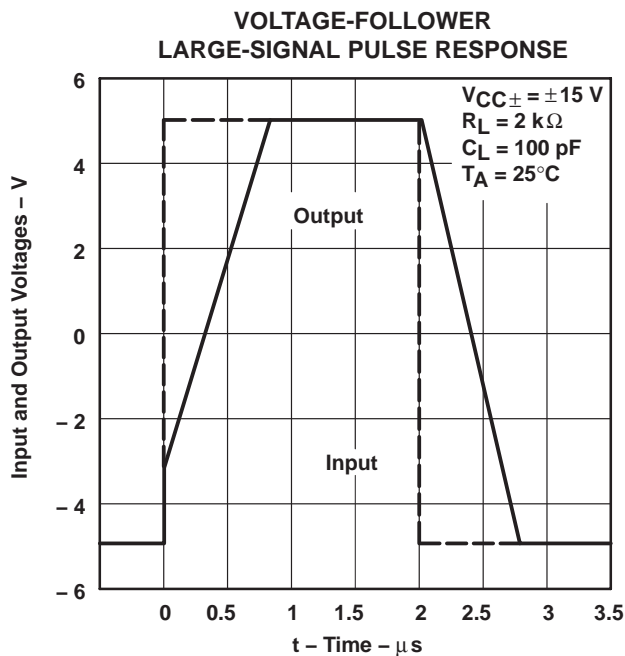


Figure 18

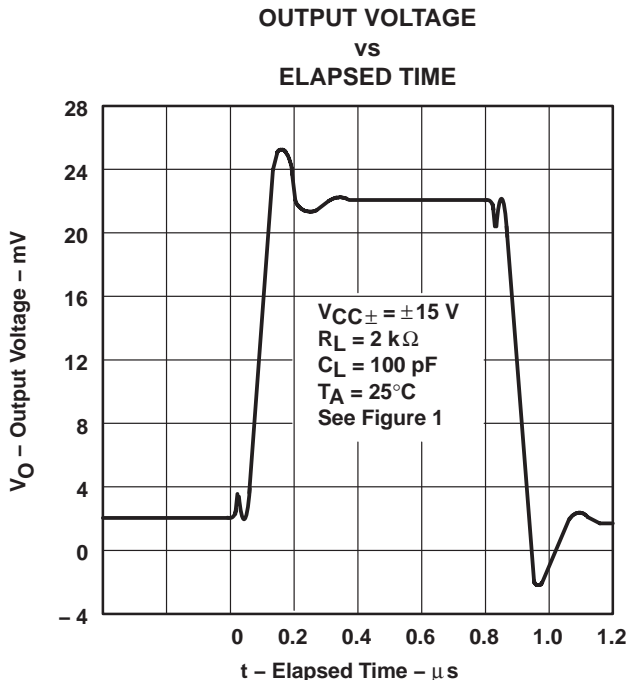


Figure 19

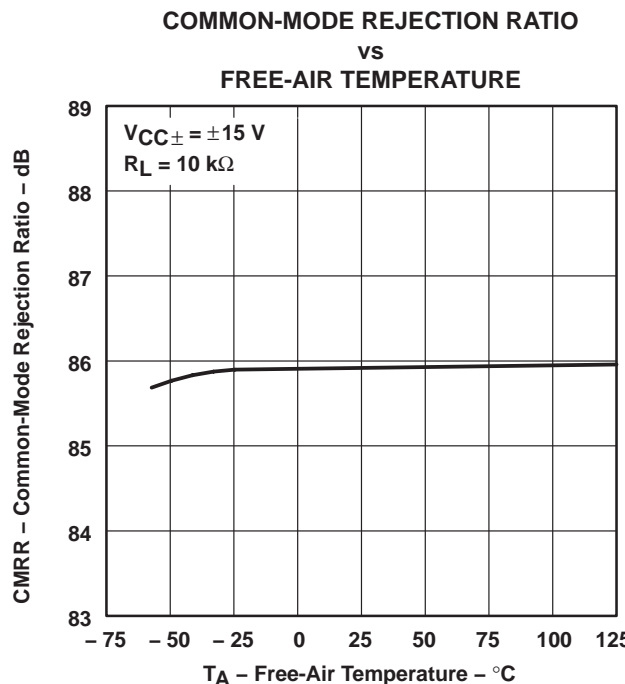


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

**TL081, TL081A, TL081B, TL082, TL082A, TL082B
TL084, TL084A, TL084B
JFET-INPUT OPERATIONAL AMPLIFIERS**

SLOS081G – FEBRUARY 1977 – REVISED SEPTEMBER 2004

TYPICAL CHARACTERISTICS†

**EQUIVALENT INPUT NOISE VOLTAGE
VS
FREQUENCY**



Figure 21

**TOTAL HARMONIC DISTORTION
VS
FREQUENCY**



Figure 22

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

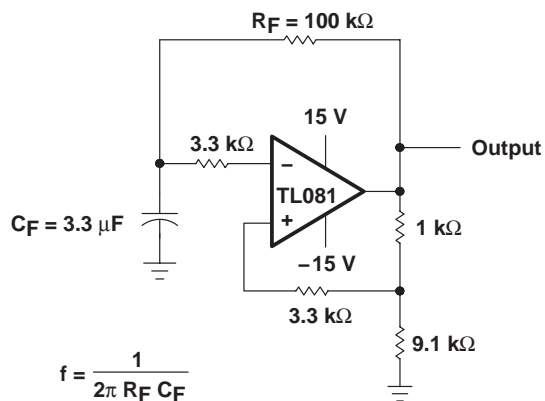


Figure 23

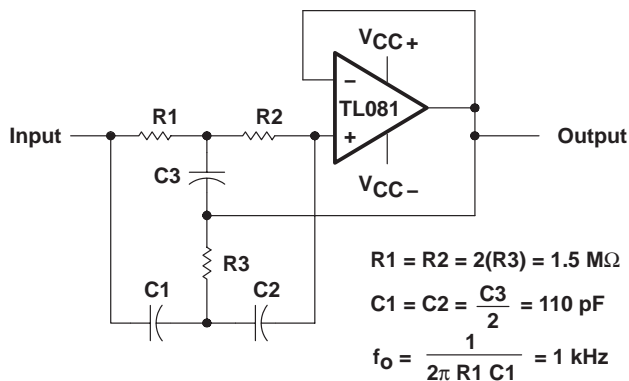


Figure 24

APPLICATION INFORMATION

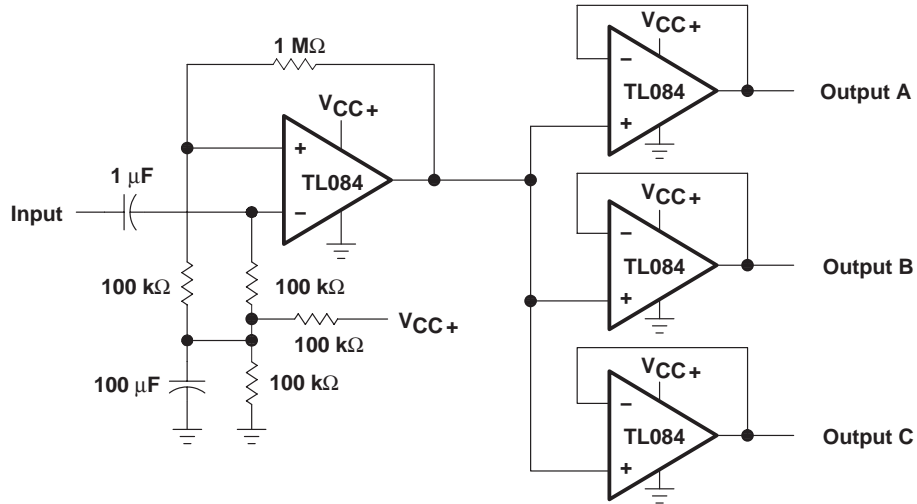


Figure 25. Audio-Distribution Amplifier



NOTE A: These resistor values may be adjusted for a symmetrical output.

Figure 26. 100-KHz Quadrature Oscillator

APPLICATION INFORMATION

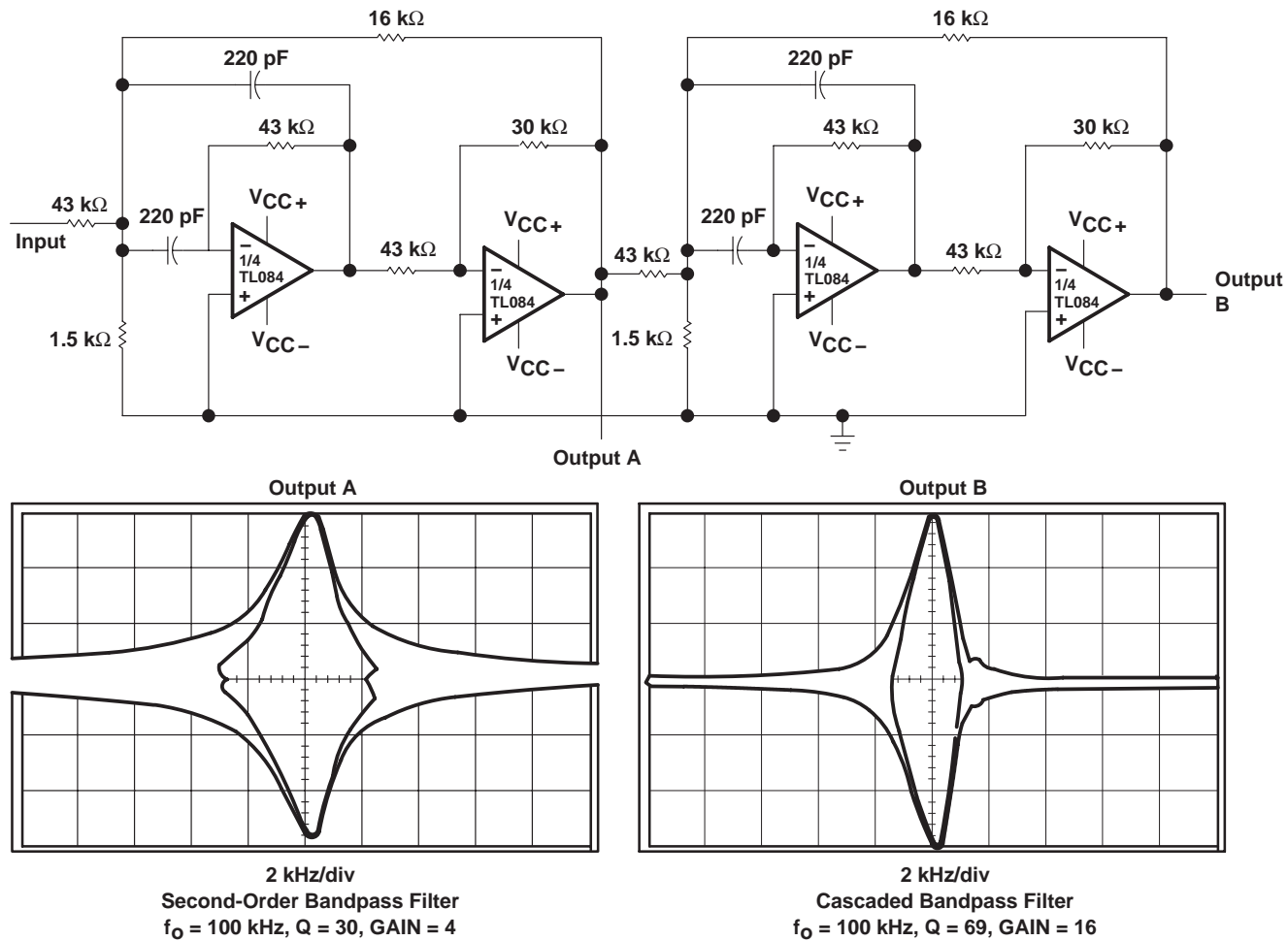


Figure 27. Positive-Feedback Bandpass Filter

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9851501Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
5962-9851501QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
5962-9851503Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
5962-9851503QCA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
TL081ACD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL081ACDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL081ACJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL081ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL081BCD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL081BCDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL081BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL081CD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL081CDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL081CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL081CPSR	ACTIVE	SO	PS	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL081CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TL081ID	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL081IDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL081IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL081MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
TL081MJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL081MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL082ACD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL082ACDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL082ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL082ACPSR	ACTIVE	SO	PS	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL082BCD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL082BCDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL082BCP	ACTIVE	PDIP	P	8	50	Pb-Free	CU NIPDAU	Level-NC-NC-NC

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
						(RoHS)		
TL082CD	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL082CDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL082CJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL082CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL082CPSR	ACTIVE	SO	PS	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL082CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL082CPW	ACTIVE	TSSOP	PW	8	150	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL082CPWE4	ACTIVE	TSSOP	PW	8	150	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL082CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TL082CPWR	ACTIVE	TSSOP	PW	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL082ID	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL082IDR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL082IJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI
TL082IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL082IPWR	ACTIVE	TSSOP	PW	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL082IPWRE4	ACTIVE	TSSOP	PW	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL082MFK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
TL082MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
TL082MJG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
TL082MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	Level-NC-NC-NC
TL084ACD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL084ACDR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL084ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL084ACNSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL084BCD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL084BCDR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL084BCN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL084CD	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TL084CDR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL084CJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
TL084CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL084CNSLE	OBSOLETE	SO	NS	14		TBD	Call TI	Call TI
TL084CNSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
TL084CNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL084CPW	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL084CPWE4	ACTIVE	TSSOP	PW	14	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL084CPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI
TL084CPWR	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL084CPWRE4	ACTIVE	TSSOP	PW	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
TL084ID	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL084IDR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
TL084IJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI
TL084IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
TL084MFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
TL084MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
TL084MJ	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
TL084MJB	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	Level-NC-NC-NC
TL084QD	ACTIVE	SOIC	D	14	50	TBD	CU NIPDAU	Level-1-220C-UNLIM
TL084QDR	ACTIVE	SOIC	D	14	2500	TBD	CU NIPDAU	Level-1-220C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

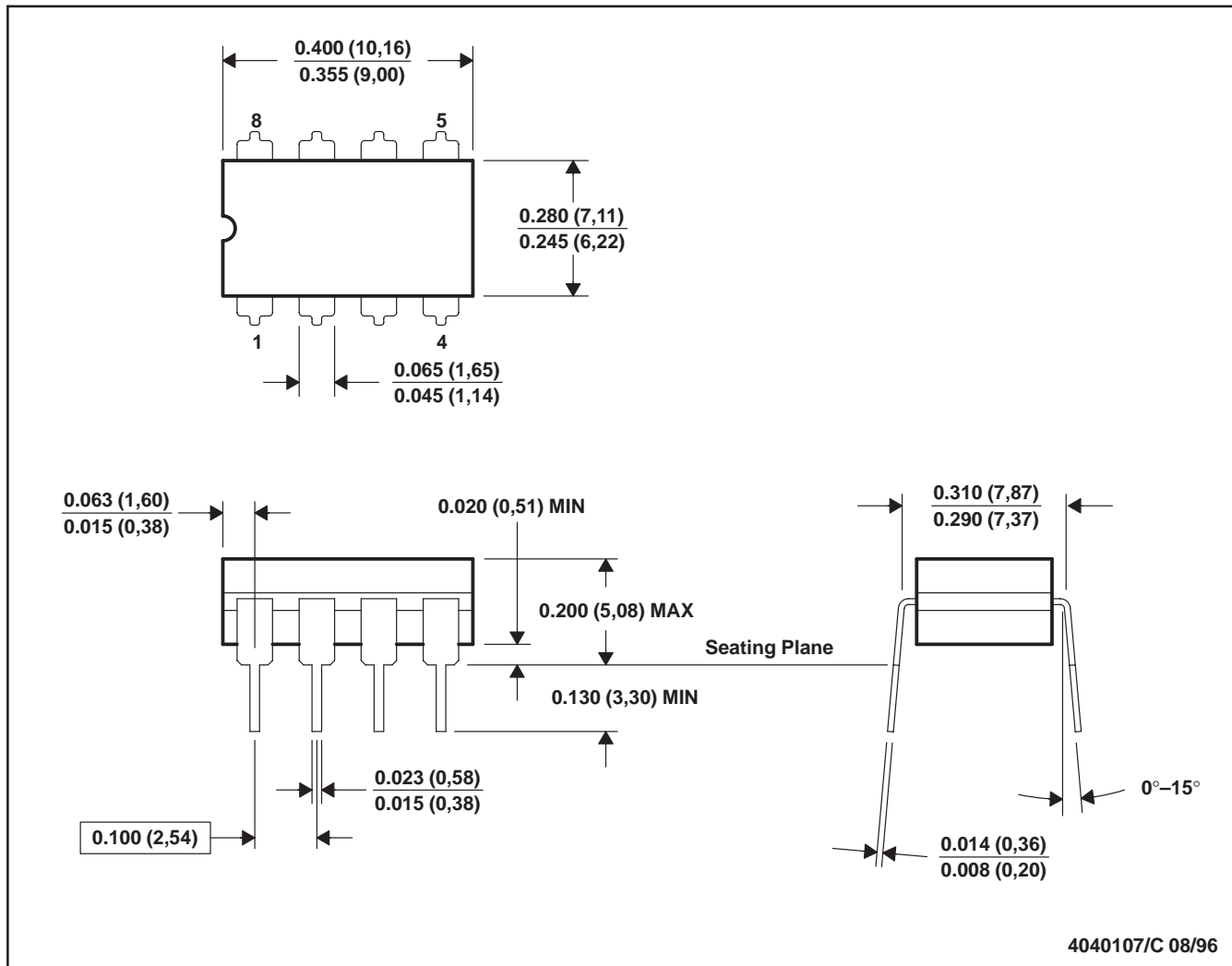
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

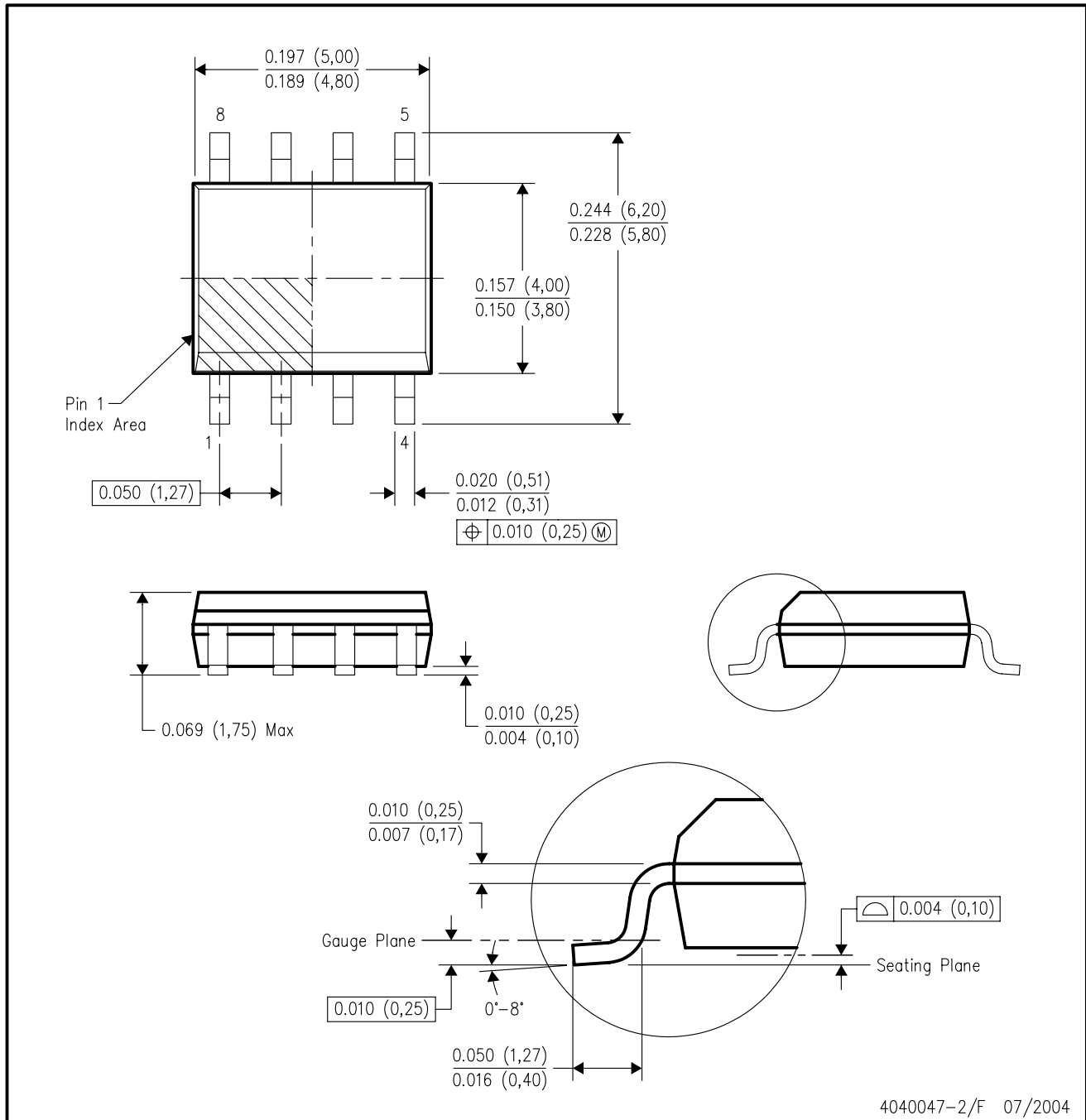
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AA.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265